

FIG. 1 (PRIOR ART)

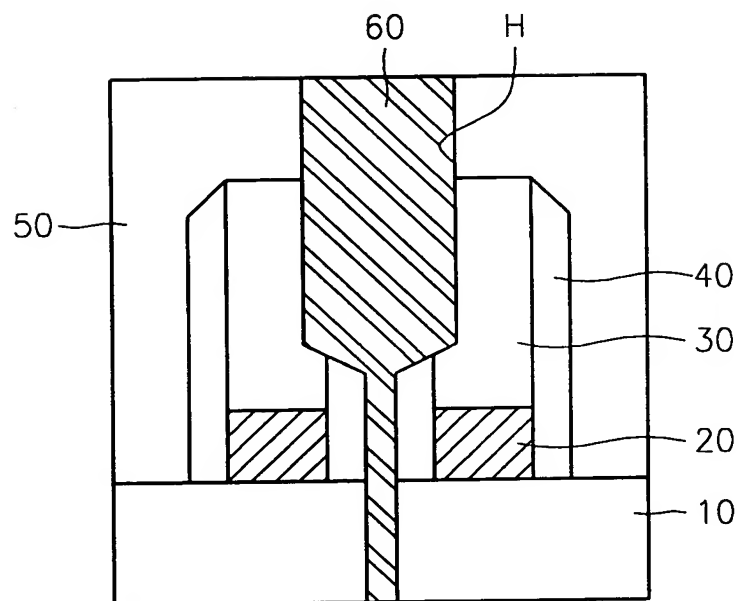


FIG. 2 (PRIOR ART)

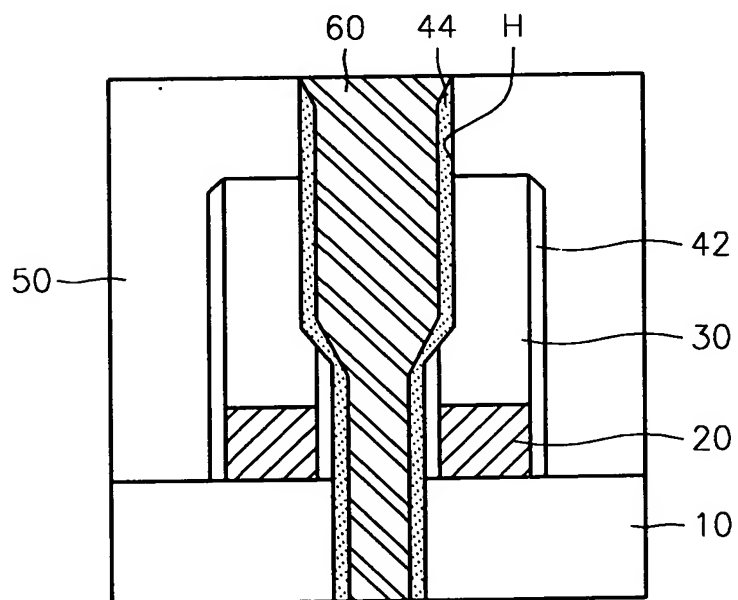


FIG. 3 (PRIOR ART)

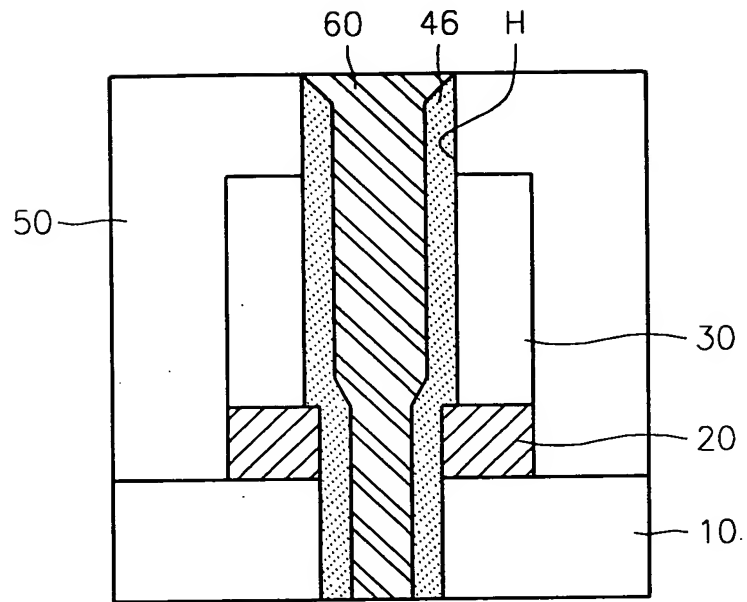


FIG. 4

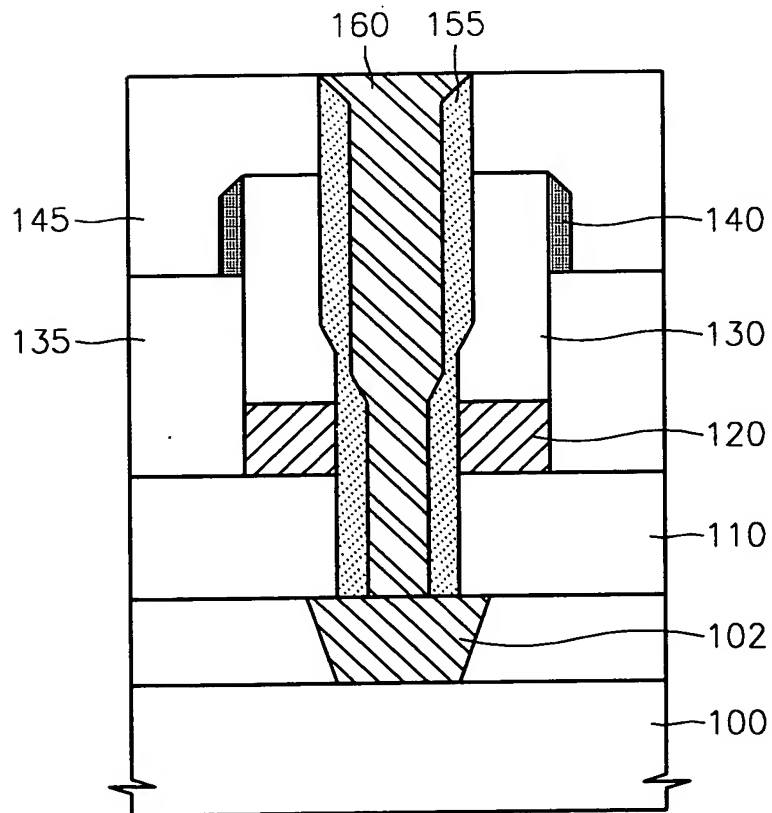


FIG. 5

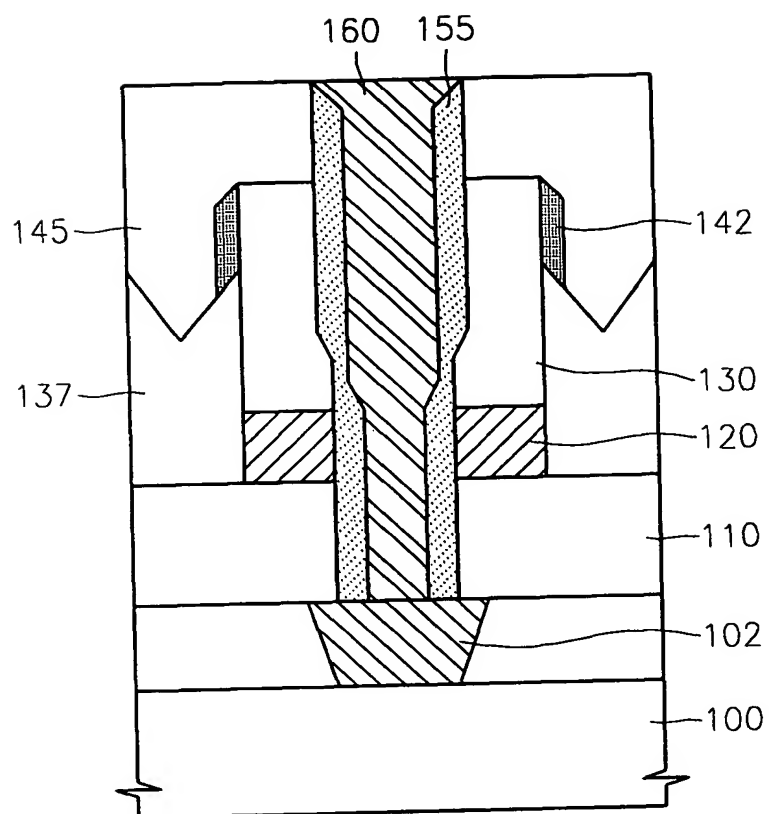


FIG. 6

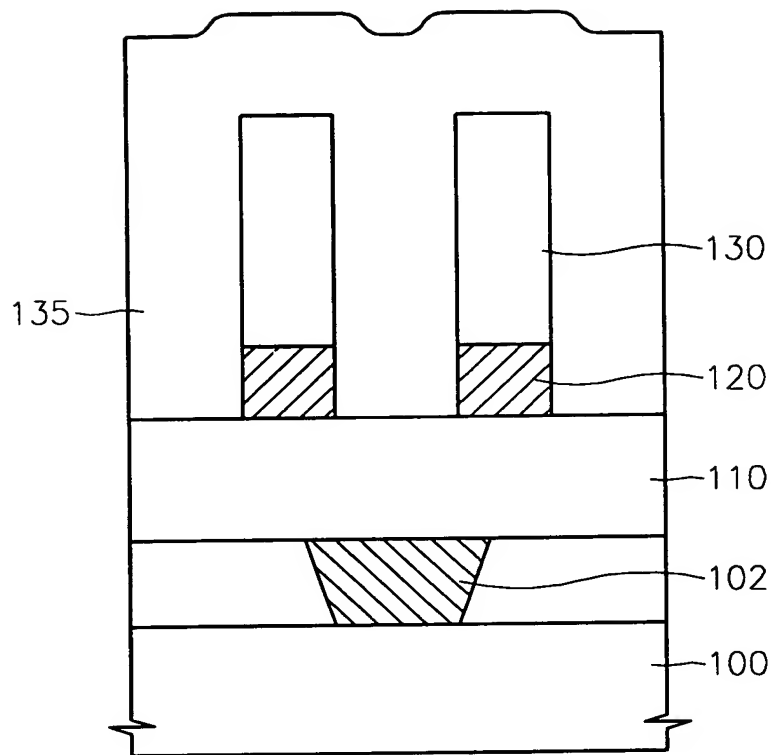


FIG. 7

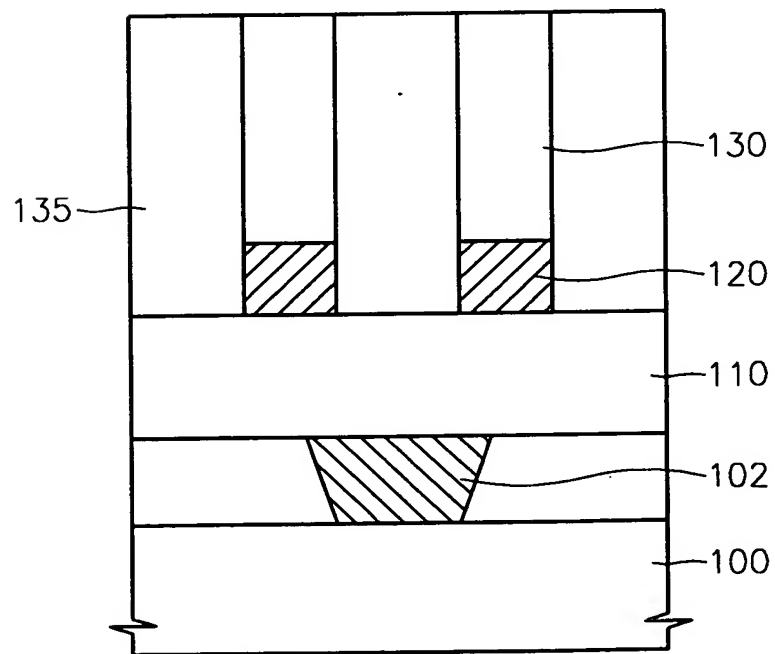


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100, a gate layer 110, a gate electrode 120, and a gate insulating layer 130. A gate insulating layer 135 is also shown on the side of the gate electrode 120.

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100, a buried layer 102, a gate stack 110, a gate electrode 135, a gate spacer 120, and a gate cap 140. The gate stack 110 is formed on the substrate 100, and the gate electrode 135 is formed on the gate stack 110. The gate spacer 120 is formed on the side of the gate stack 110, and the gate cap 140 is formed on top of the gate stack 110.

FIG. 10

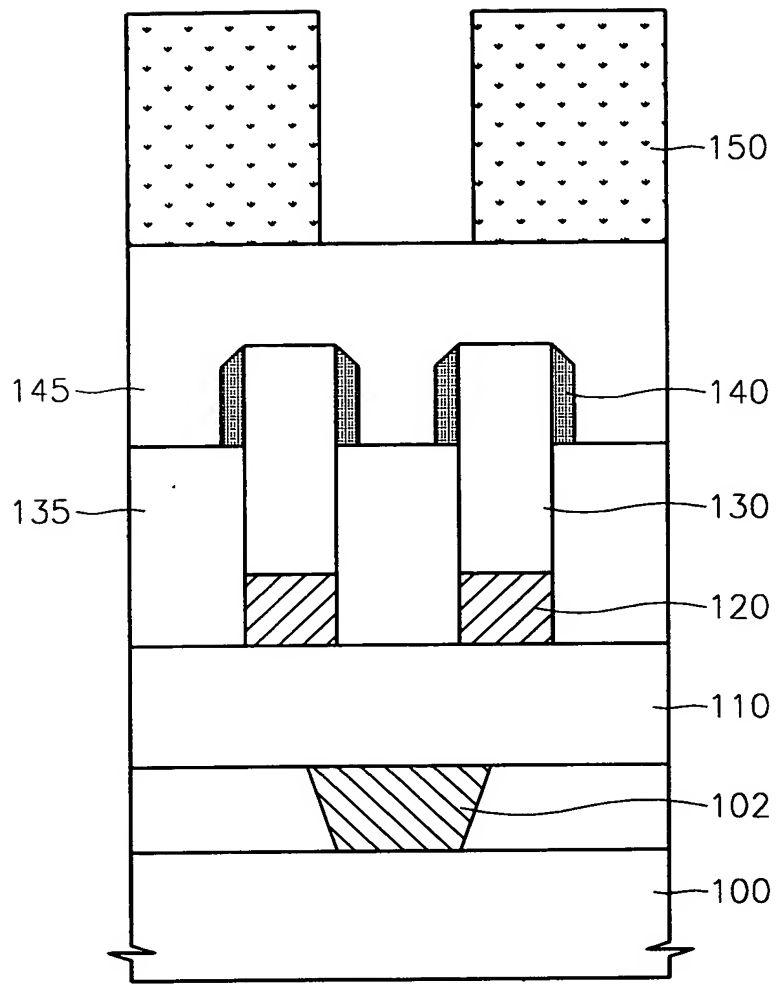


FIG. 11

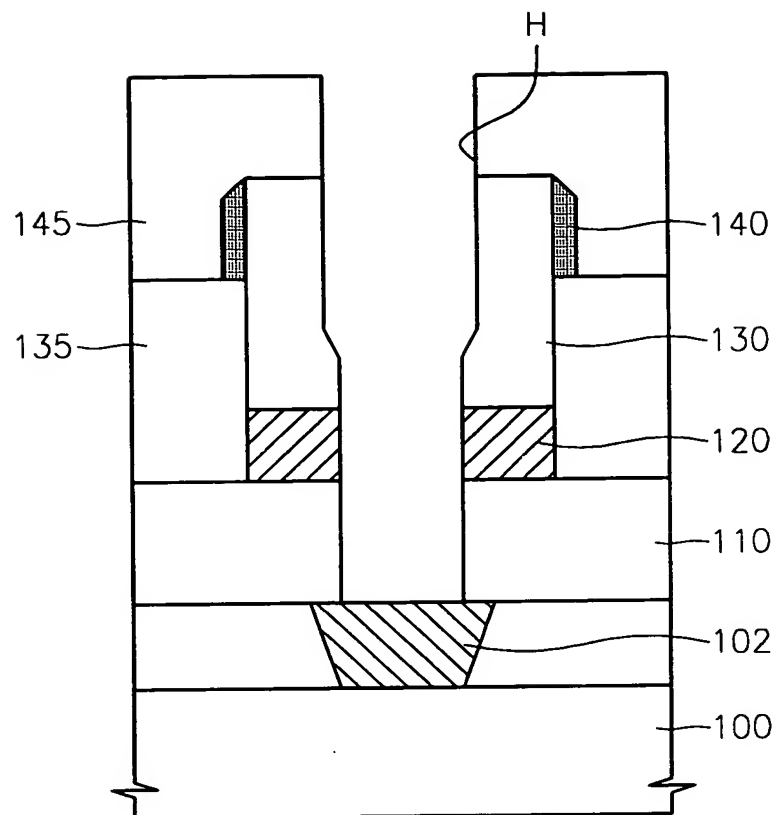


FIG. 12

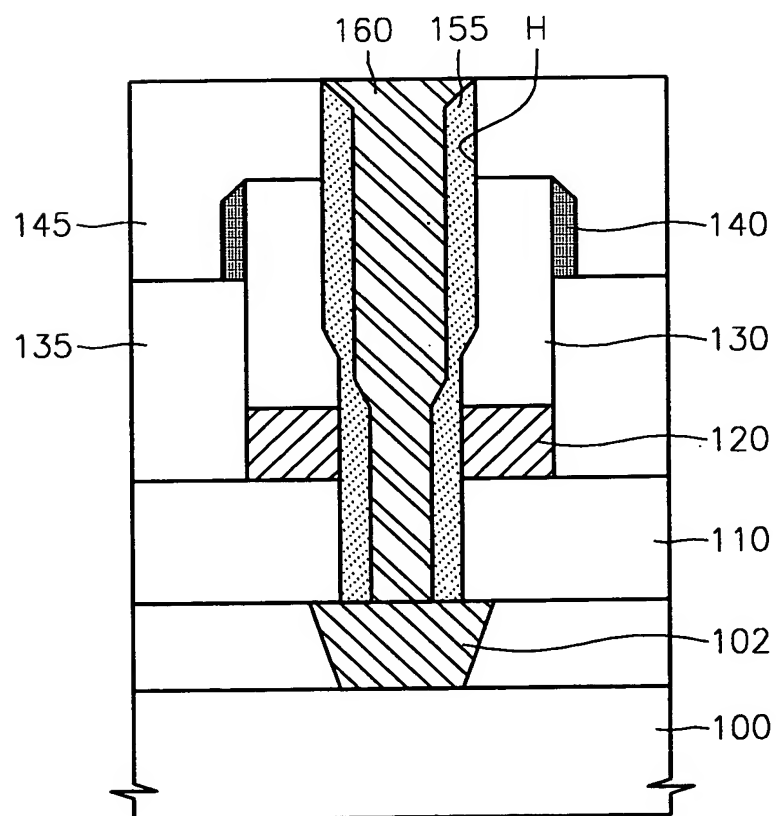


FIG. 13

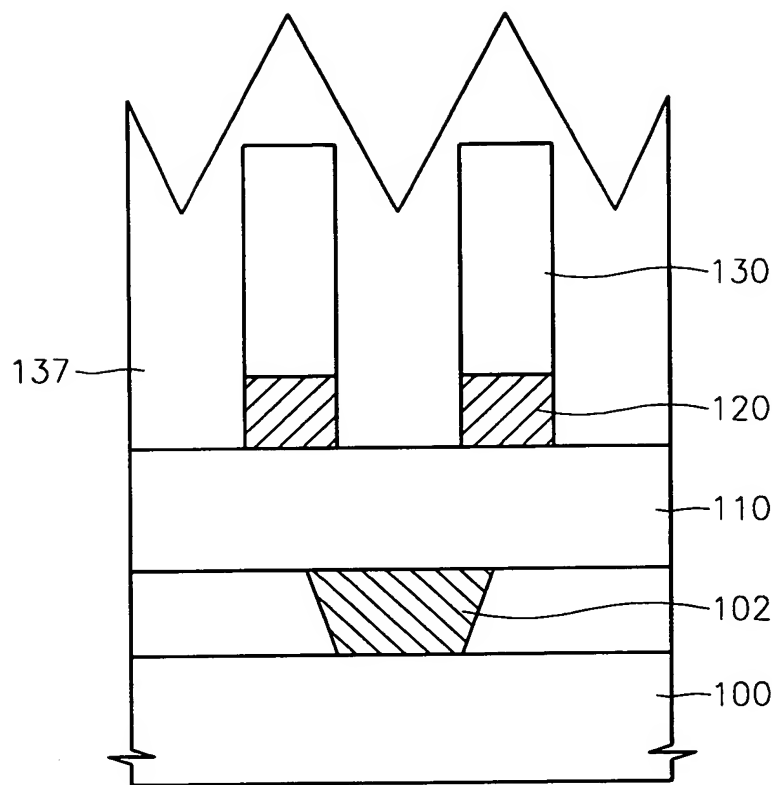


FIG. 14

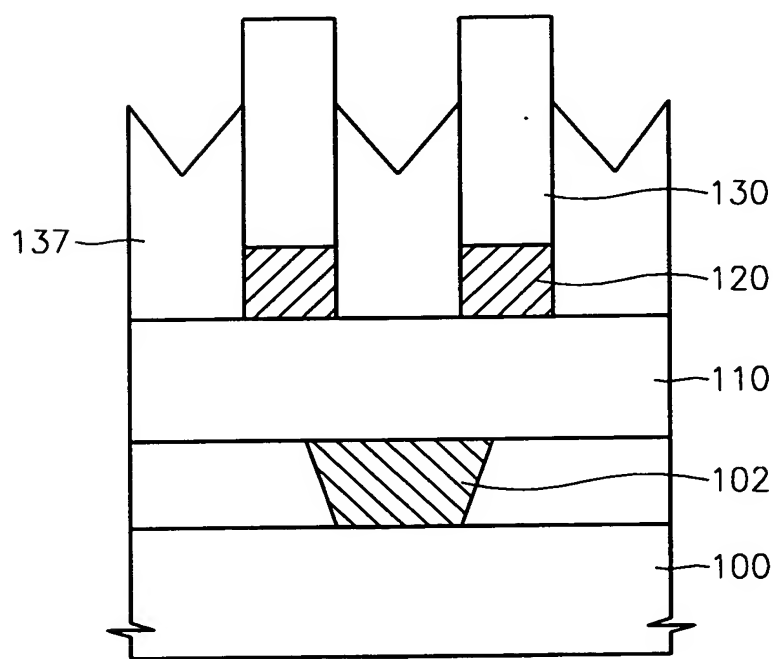


FIG. 15

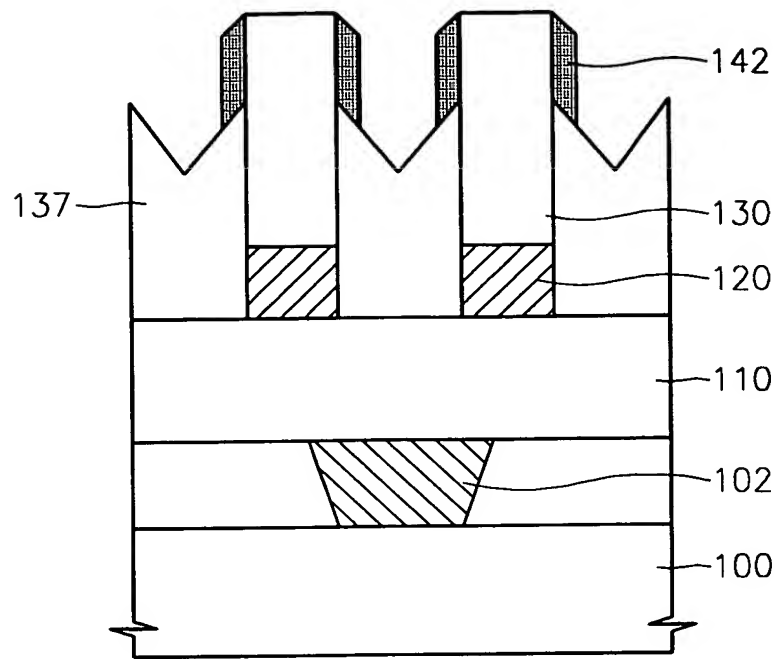


FIG. 16

